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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/817,632	04/02/2004	Anders Landin	5181-95501	2854

35690 7590 10/20/2006

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EXAMINER	
DOAN, DUC T	

ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 10/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/817,632	LANDIN ET AL.	
	Examiner	Art Unit	
	Duc T. Doan	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 September 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,7,8,10-14 and 16-20* is/are rejected.

7)☒ Claim(s) *6,15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Status of Claims

Claims 1-20 have been presented for examination in this application. In response to the last office action, claims 1,10 have been amended. As the result, claims 1-20 are now pending in this application.

Claims 1-5,7-8,10-14,16-20 are rejected.

Claims 6,15 are objected to.

All rejections and objections not explicitly repeated below are withdrawn.

Applicant's arguments filed 9/11/06 have been fully considered but they are mooted in view of new ground(s) of rejection necessitated by the Applicant's amendments to the claims.

Claim Objections

Claims 1,10 objected to because of the following informalities:

As in claims 1,10, line 1, "(Original)" should be replaced with "(Currently amended)". Appropriation correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-5,7-8,10-14,16-20 rejected under 35 U.S.C. 103(a) as being unpatentable over Chi et al (US 5940870) in view of Ang (US 6678799).

As in claim 1, Chi A system, comprising: a plurality of nodes, wherein each node includes an active device and a memory subsystem coupled to the active device (Chi's Fig 4: memory subsystem, #54 cluster cache, #43 memory controller, #62 private memory, #64 global memory) ; wherein an active device in a node of the plurality of nodes is configured to generate a global address and translation information identifying a translation function (Chi's Fig 8: device configured to generate global address), wherein the global address identifies a coherency unit (global address is used to identify coherency memories in nodes);

wherein a memory subsystem included in the node is configured to perform the translation function identified by the translation information on the global address to generate a physical address of the coherency unit within the memory subsystem (Chi's Fig 8, global address is used by the destination node to generate physical address of physical memories in destination node, Fig 7 further shows the mapping to destination node physical memory #100);

wherein an additional memory subsystem included in an additional node of the plurality of nodes is configured to store the translation information identifying the translation function used in the node (Chi's Fig 8, column 5 lines 27-46 discloses data structures in each node to store the translation information that identifying the translation function used in each node, such as Fig 8: node ID #114, #110 partition number, ATM tables and indexes), wherein in response to

a request for access to the coherency unit, the additional memory subsystem is configured to send the translation information to the node.

Chi's column 6 lines 21-25 discloses that a transaction packet including information in the global address such as the "translation information" (Chi's Fig 8: node ID, Partition, ATM indexes) destined to another node is generated and sent to a remote/destination node. Chi does not expressly disclose the claim's aspect of the additional memory subsystem is configured to send the translation information to the node. However, Ang's column 5 lines 27-30 discloses a distributed shared cached memory system in multiple nodes (Fig 1), in which the home node (Ang's Fig2: node 3) for a coherency unit has a directory keep tracks all necessary meta data and status for a cache line. When a request/packet for a cache line arrived, the home node's directory is consulted, and the home node (corresponding the claim's another node) sends out the response packet, including the address and node ID identifying the location an the manner the data being cached (Ang's column 5 lines 19-26). It would have been obvious to one of ordinary skill in the art at the time of invention to include the home node as suggested by Ang in Chi's system thereby the location and manner of data being cached car readily provided by the home node in the situation wherein the data is not cached at the requesting node (Ang's column 5 lines 13-21; 27-36).

As in claim 2, the claim recites wherein the plurality of nodes are coupled by an inter-node network, and wherein each of the plurality of nodes includes an interface to the inter-node network (Chi's Fig 1: #20 internode network); wherein an additional interface included in the additional node is configured to receive the translation information for the coherency unit from

the additional memory subsystem (Chi's Fig 8 shows destination node receiving the translation information for a coherence memory cached data) ;

wherein the additional interface is configured to provide the translation information and the global address to an interface included in the node via the inter-node network; and wherein the interface included in the node is configured to provide the translation information and the global address received via the inter-node network to the memory subsystem. The claim rejected based on the same rationale of claim 1 (Aug further discloses the home node's directory is consulted, and the home node (corresponding the claim's another node) sends out the response packet, including the address and node ID identifying the location an the manner the data being cached (Ang's column 5 lines 19-26)).

As in claim 3, the claim recites wherein the additional memory subsystem is configured to perform a different translation function on the global address to obtain a local physical address of the coherency unit within the additional memory subsystem (Chi's column 6 lines 25-35 discloses that the destination node translates the global address to its local space memory).

As in claim 4, the claim recites wherein the additional memory subsystem is configured to store translation information associated with the coherency unit for several other nodes included in the plurality of nodes, wherein different translation information is associated with each of the several other nodes (Ang's column 7 lines 3-9 discloses the directory at the home node store/maintain information for addresses that are cached at multiple other nodes).

As in claim 5, Chi's column 5 lines 1-10 discloses wherein each active device included in the plurality of nodes is configured to use at least a portion of the global address of the coherency unit to determine whether a copy of the coherency unit is locally cached by that active device.

As in claim 7, the claim recites wherein no memory subsystem included in an other node of the plurality of nodes maps the global address, wherein an other active device included in the other node is configured to request access to the coherency unit by sending a packet including the global address and translation information associated with the coherency unit in the other node on a network included in the other node, wherein the translation information associated with the coherency unit in the other node indicates that no memory subsystem included in the other node maps the coherency unit. The claim appears to describe the situation, a source processor in the source node (active device in an other node) having a cache miss (no memory subsystem .. maps the global address), it generates the global address and sending out a request/packet to a destination processor in the same other node. Chi's Fig 7, column 5 lines 1-10 discloses the global address is generated by the source processor and sending to the destination processor via the processor bus, within the local space, in the same node.

As in claim 8, the claim recites wherein an other interface included in the other node and coupled to the network is configured to forward the global address to an additional interface included in the additional node in response to receiving the packet (Chi's Fig 1 shows in a ring topology, the packet can be forwarding from one node to another).

Claim 10 rejected based on the same rationale as of claim 1.

Claim 11 rejected based on the same rationale as of claim 2.

Claim 12 rejected based on the same rationale as of claim 3.

Claim 13 rejected based on the same rationale as of claim 4.

Claim 14 rejected based on the same rationale as of claim 5.

Claim 15 rejected based on the same rationale as of claim 6.

Claim 16 rejected based on the same rationale as of claim 7.

Claim 17 rejected based on the same rationale as of claim 8.

Claim 18 rejected based on the same rationale as of claim 9.

As in claim 19, the claim recites an operating system executing on the active device creating a translation lookaside buffer entry corresponding to the virtual address, wherein the translation lookaside buffer entry includes the global address and the information identifying the translation function, wherein the operating system selects the translation function in order to map the global address to the local physical address within the memory. Chi's column 3 lines 30-45 disclose a translation table with entries includes global address and translation function as shown in Fig 8.

As in claim 20, the claim recites an operating system executing on the active device in the node creating a translation lookaside buffer entry corresponding to a virtual address in response to deciding to replicate the coherency unit to the node from the additional node, wherein the translation lookaside buffer entry corresponding to the virtual address specifies the global address and the information identifying the translation function. The claim rejected based on the same rationale of claim 19. Chi's column 6 lines 21-28 further discloses the translation is filled by operating system when an application to be run on the system.

Claim 9 rejected under 35 U.S.C. 103(a) as being unpatentable over Chi et al (US 5940870), in view of Ang (US 6678799) as applied to claim 1 and further in view of Arimili et al (US 2002/0112124).

As in claim 9, the claim recites wherein a memory controller included in the memory subsystem is integrated in a same integrated circuit as the processing subsystem. Chi does not describe the claim's aspect of integrated memory controller. However, Arimilli's paragraph 6 discloses a multiple processors system with integrated memory controller circuit. It would have been obvious to one of ordinary skill in the art at the time of invention to include integrated memory controller circuit as suggested by Arimilli in Chi's system to allow fast communication between the processor and the memory controller since they are located in the same chip. (Arimilli's page 1 paragraph 6).

Allowable Subject Matter

Claims 6,15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

When responding to the office action, Applicant is advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist examiner to locate the appropriate paragraphs.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Duc T. Doan whose telephone number is 571-272-4171. The examiner can normally be reached on M-F 8:00 AM 05:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on 571-272-4210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DD

Mano Padmanabhan 10/15/06

MANO PADMANABHAN
SUPERVISORY PATENT EXAMINER